(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 January 2004 (29.01.2004)

PCT

(10) International Publication Number
WO 2004/010317 A1

(51) International Patent Classification[7]: G06F 13/40

(21) International Application Number:
PCT/US2003/022943

(22) International Filing Date: 23 July 2003 (23.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/205,664 24 July 2002 (24.07.2002) US

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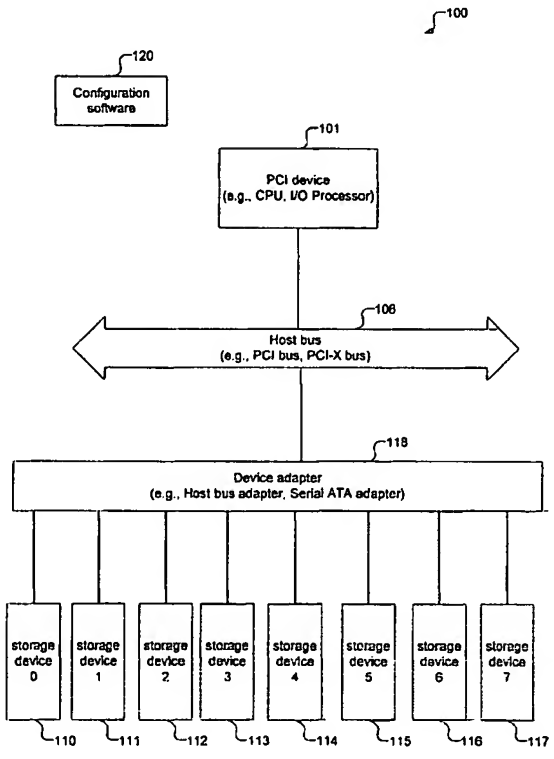
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: METHOD, SYSTEM, AND PROGRAM FOR CONTROLLING MULTIPLE INPUT/OUTPUT DEVICES



(57) Abstract: Provided are a method, system and article of manufacture for controlling one or more I/O devices coupled to a local bus. A local bus function is associated with the one or more I/O devices. A register corresponding to the local bus function is configured as a memory address. The one or more I/O devices are controlled via the configured register.

WO 2004/010317 A1

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

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METHOD, SYSTEM, AND PROGRAM FOR CONTROLLING MULTIPLE INPUT/OUTPUT DEVICES

BACKGROUND OF THE INVENTION

1. Field of the Invention

1[] The present invention relates to a system, method, and program for controlling multiple storage devices.

2. Description of the Related Art

2[] A local input/output (I/O) bus is a high-speed input/output (I/O) bus used for coupling peripheral devices, such as storage devices, to a computer system. The Peripheral Component Interconnect (PCI) bus and enhancements to the PCI bus, such as the PCI-X bus, are the commonly used I/O buses.

3[] A PCI physical device is a physical device that may be coupled to the PCI bus. Each PCI physical device may incorporate from one to eight separate PCI functions. A PCI function may be a logical device. Each PCI function may include a configuration header that may be configured to control peripheral devices coupled to the PCI bus. The configuration header may include configuration registers, such as base address registers. Six base address registers comprising base address register 0 (BAR0), base address register 1 (BAR1), base address register 2 (BAR2), base address register 3 (BAR3), base address register 4 (BAR4), base address register 5 (BAR5) may be present in the configuration header. Each base address register may be 32 bits, i.e., a dword. Further details of the PCI bus (i.e., the PCI specification) are described in the publication entitled "PCI Local Bus Specification" by the PCI Special Interest Group (Revision 2.2, Copyright 1992, 1993, 1995, 1998 PCI Special Interest Group) and base address registers are described in Chapter 6 of the PCI specification.

4[] A device adapter, such as a host bus adapter (HBA), may act as the interface between the PCI/PCI-X bus and the storage devices. The interface can control the transfer of data from a computer to a storage device and vice versa. Interfaces for storage disks include the Integrated Drive Electronics (IDE) interface (known also as an Advanced Technology Attachment interface, i.e., ATA, interface) and the Serial ATA (SATA) interface. Further details of SATA are described in the publication entitled "Serial ATA: High Speed Serialized AT attachment" by the Serial ATA Working Group (Revision 1.0, Copyright

2001). Technologies analogous to IDE/ATA such as the ATA packet interface (ATAPI) are available for CD ROM and DVD drives. The bandwidth and processing capabilities of the interface can substantially affect system performance, system configuration, system compatibility, system upgradability, etc.

5[] A channel is typically the data pathway over which information flows in the IDE interface. As per the PCI IDE interface there may be two channels, primary channel and secondary channel, per PCI function. Furthermore, each channel can support at most two devices. For example, the primary channel can supports two IDE storage devices and the secondary channel can support two IDE storage devices. The configuration header of the PCI function may be configured to control four PCI IDE devices attached to the PCI bus. BAR0, BAR1, BAR2, BAR3 and BAR4 may be configured as I/O BARs. I/O BAR0 may be the command register block for the primary channel. I/O BAR1 may be the control register block for the primary channel. I/O BAR2 may be the command register block for the secondary channel. I/O BAR3 may be the control register block for the secondary channel. I/O BAR4 may provide control for bus master registers for both the primary channel and the secondary channel. BAR5 may be device specific, i.e., BAR5 is not part of the PCI IDE specification. Hence, a single PCI function can control at most four IDE storage devices via the two channels. Configuring the BARs as I/O BARs for PCI IDE is described in the publication entitled "PCI IDE Controller Specification" (Revision 1.0, 1994) in pages 1-5.

6[] Although in the prior art PCI IDE/ATA has been used for supporting peripheral devices, there is a need in the art for improved techniques for controlling peripheral devices in a local I/O bus architecture with interfaces such as the SATA.

BRIEF DESCRIPTION OF THE DRAWINGS

7[]

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIG. 1 illustrates a bus architecture for accessing data in storage devices in accordance with certain described embodiments of the invention;

FIG. 2 illustrates a block diagram for a PCI function for devices in accordance with certain described embodiments of the invention;

FIG. 3 illustrates a block diagram of a configuration header of a PCI function for point-to-point connectivity in accordance with certain described embodiments of the invention; and

FIG. 4 illustrates logic for controlling storage devices attached to a local bus in accordance with certain described embodiments of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

8[] In the following description, reference is made to the accompanying drawings which form a part hereof and which illustrate several embodiments of the present invention. It is understood that other embodiments may be utilized and structural and operational changes may be made without departing from the scope of the present invention.

9[] Described embodiments of the invention provide techniques to allow a single PCI function to control more than four ATA/ATAPI/SATA devices. Additional embodiments of the invention enable a switch between a PCI IDE mode in which no more than four devices can be controlled using a single PCI function and a direct address mode in which more than four ATA/ATAPI/SATA devices can be controlled using a single PCI function.

10[] FIG. 1 illustrates a system 100, including a bus architecture for accessing data in storage devices, such as SATA storage devices, in accordance with embodiments of the invention. A PCI device, such as a central processing unit (CPU) or an I/O processor, 101 is coupled to a host bus, such as a PCI (or a PCI-X) bus 106. The CPU may be any CPU known in art such as the INTEL** x86 family of microprocessors, the PowerPC** processor, etc. The I/O processor may comprise any I/O processor known in the art such as the INTEL** 80321 or the INTEL** 80310.

11[] Eight storage devices, such as storage devices 110...117 are coupled to the PCI bus 106 via a device adapter, such as an Serial ATA (SATA) adapter, 118. The storage devices 110...117 may be any type of storage device known in the art, such as an SATA, ATA, ATAPI, etc., type of storage devices. The device adapter 118 may be any type of device adapter known in the art, such as SATA, ATA, ATAPI, etc., type of storage adapters. While eight storage devices 110...117 are shown, a lesser or greater number of storage devices may be connected to the PCI bus 106 via the device adapter 118.

12[] The device adapter 118 couples each of the eight storage devices 110...117 to the PCI bus 106 with their own respective cables in a point-to-point fashion. Thus each of the eight storage devices 110...117 may transfer data simultaneously in a direct access mode.

13[] Configuration software 120 can configure the system 100 such that the devices 110...117 can exchange data via the PCI bus 106. The configuration software 120 may be part of a BIOS, be part of a standalone software module, be part of device drivers resident on the system 100, be coupled to the PCI device 101, etc.

14[] FIG. 2 illustrates a block diagram indicating a representative number of storage devices controllable by a single PCI function 200 corresponding to the system 100, in accordance with embodiments of the invention. In FIG. 2, the single PCI function 200 can control the eight storage devices 110...117 in accordance with embodiments of the invention. In alternative embodiments of the invention a lesser or a greater number of devices may be controllable by the single PCI function 200. The PCI function 200 implements a base set of configuration registers 202 defined in chapter 6 of the PCI specification. The configuration registers 202 are part of a configuration space (not shown in FIG. 2) that are associated with the PCI function 200 as per the PCI specification. The embodiments of FIG. 1 and FIG. 2 may allow for more than four devices to be simultaneously coupled to the PCI bus per PCI function. Furthermore because of the point-to-point connectivity of the storage devices 110...117, each of the storage devices 110...117 can transfer data simultaneously.

15[] The PCI device 101 may possess the ability to address two distinct address spaces: I/O and memory. The PCI device 101 use PCI I/O and memory transactions to access PCI I/O and memory locations, respectively. In addition, a third access type, the configuration access, is used to access a device's configuration registers.The configuration registers 202 of the PCI function 200 may be initialized at the reset time of system 100 to configure the PCI function 200 to respond to memory and I/O address ranges assigned to the PCI function by the configuration software 120.

16[] When a system, such as system 100 is reset, configuration software, such as the configuration software 120, scans the various buses in the system 100 to determine what devices exist and what configuration requirements they have. The process is referred to as "scanning the bus" or "walking the bus." The configuration registers 202 (illustrated in FIG. 2) defined in Chapter 6 of the PCI specification are implemented in order to facilitate this process.

17[] FIG. 3 illustrates a configuration header 300 of the PCI function 200 for point to point connectivity of the storage devices 110...117 to the PCI bus 106, in accordance with certain embodiments of the invention.

18[] In FIG. 3, the two 32-bit base address registers BAR0 and BAR1 are together configured as a 64 bit memory base address register (memory BAR indicated by reference numeral 302) starting at address 10hex. In alternative embodiments a different starting address different from 10hex can be used to store the memory BAR 302. In FIG. 3, the dwords 306, 308, 310, 312, corresponding to the base address registers BAR2, BAR3, BAR4, and BAR5 respectively, may be left unused. The register set of the storage devices 110...117 may be mapped into memory space by the memory BAR 302. In certain embodiments the memory BAR 302 may be 64 bits long, and may locate an address in a 2^{64} bit memory space, wherein areas of the memory space correspond to regions used to control the storage devices 110...117. The storage devices 110...117 may be controlled by accessing the memory space.

19[] Therefore, the memory BAR 302 implements a "programmable memory decoder" in the PCI function 200. The configuration software 120 can assign a 64-bit memory address within the memory space to the memory BAR 302. Since the memory BAR 302 may be 64 bits long the total amount of addressable memory may be 2^{64} bytes, which is large enough to map the register set of the storage devices 110...117. In one embodiment of the invention, the amount of memory space required to control each of the storage devices 110...117 is at most 512 bytes. With 512 bytes per storage device, the number of storage devices, such as storage disks, that may be connected to the PCI bus 106 via the use of the memory BAR 302 is significantly greater than four. In alternative embodiments, the amount of memory space required to control each storage device 110...117 is a greater or lesser number of bytes. The number of bytes required per storage device is guided by the capabilities needed to control each device and is a function of the feature set to be supported for each device. In view of the large addressable space in the memory BAR 302 and the relatively small number of bytes required per storage device, the number of storage devices that can be supported simultaneously in embodiments of the invention for SATA connectivity is very large. Hence, embodiments of the invention provide configuration mechanisms such that the system 100 is able to convert accesses initiated by a CPU or an I/O processor comprising the PCI device 100, with certain predefined addresses into configuration access on the PCI bus 106, where more than four ATA/ATAPI/SATA devices are connected to the PCI bus 106.

20[] FIG. 4 illustrates logic for controlling storage devices attached to the local bus 106 in accordance with described embodiments of the invention. The logic described in FIG. 4

may be performed by configuration software, such as configuration software 120, where the configuration software 120 is coupled to a system in which storage devices may be connected to a local bus in either a point-to-point scheme such as in system 100 or in a prior art daisy chained scheme, such as in a PCI IDE mode.

21[] At block 400, the system 300 is reset. Control proceeds to block 404, where the configuration software 120 determines whether storage devices attached to the system are in PCI IDE mode. If so, control proceeds to block 408 where the configuration software 120 configures the base address registers as I/O base address registers in a manner known in prior art and the process stops (at block 412).

22[] If at block 404, the configuration software 120 determines that storage devices attached to the system are not in PCI IDE mode control proceeds to block 416 where configuration software 120 determines whether the storage devices connected to the PCI bus 106 are in a direct access mode (i.e., the storage devices are connected to the PCI bus in a point-to-point scheme, e.g., in a SATA mode). If so, the configuration software 120 configures (at block 420) the base address registers 302...312 as the memory BAR 302 as described in FIG. 3, and the process stops (at block 412). As a result of configuring the memory base address register 302, more than four devices, such as the storage devices 110...117, can be attached to the PCI bus 106 in a point-to-point manner. If at block 416, the configuration software 120 determines that the storage devices are not in a direct access mode the process stops (at block 412).

23[] The logic described in FIG. 4 enables the operation of the system 100 in either the PCI IDE mode or in the mode where more than four ATA/SATA type devices can be attached to the PCI bus. The logic of FIG. 4 implements an interface where the single PCI function 200 can control the eight storage devices 110...117.

24[] Block 408, implements a configuration to control IDE/ATA devices using a PCI function, which requires the IDE/ATA devices be mapped to I/O space. This means that up to four IDE/ATA devices (or ATAPI or SATA) can be controlled simultaneously using a single PCI function. Described embodiments further provide a programming interface, utilizing memory space, which allows the control of more than four IDE/ATA/ATAPI/SATA devices using a single PCI function. Being able to use only a single PCI function versus multiple functions, reduces the amount of hardware required. Additional embodiments of the invention enable a switch between a PCI IDE mode in which no more than four devices can be controlled using a single PCI function and a direct

address mode in which more than four I/O devices can be controlled using a single PCI function.

Additional Embodiments

25[] The operations described herein may be implemented as a method, apparatus or article of manufacture using standard programming and/or engineering techniques to produce software, firmware, hardware, or any combination thereof. The term "article of manufacture" as used herein refers to machine readable instructions or logic implemented in hardware logic (e.g., an integrated circuit chip, Programmable Gate Array (PGA), Application Specific Integrated Circuit (ASIC), etc.) or a machine readable medium (e.g., magnetic storage medium (e.g., hard disk drives, floppy disks,, tape, etc.), optical storage (CD-ROMs, optical disks, etc.), volatile and non-volatile memory devices (e.g., EEPROMs, ROMs, PROMs, RAMs, DRAMs, SRAMs, firmware, programmable logic, etc.). Code in the computer readable medium is accessible and executable by a processor. The code in which preferred embodiments are implemented may further be accessible through a transmission media or from a file server over a network. In such cases, the article of manufacture in which the code is implemented may comprise a transmission media, such as a network transmission line, wireless transmission media, signals propagating through space, radio waves, infrared signals, etc. Of course, those skilled in the art will recognize that many modifications may be made to this configuration without departing from the scope of the present invention, and that the article of manufacture may comprise any information bearing medium known in the art.

26[] In the described embodiments, the storage devices communicate on a bus topology, such as a PCI-X or PCI bus topology. In alternative embodiments, the storage devices may communicate using any communication architecture known in the art. Alternative embodiments may use interfaces other than IDE, ATA, SATA or ATAPI.

27[] In PCI bus embodiments, additional PCI-X or PCI bridges may be used. In certain embodiments, the storage devices comprised magnetic hard disk drives. In alternative embodiments, the storage devices may comprise any storage device known in the art, such as optical disks, tapes, CDROM drives, DVDs etc.

28[] In the embodiments the length of registers have been illustrated with a certain number of bits. In the embodiments, if the host bus is a PCI bus, then each base address register is 32 bits wide if the base address register is an I/O decoder and may be either 32

bits or 64 bits wide if the base address register is a memory decoder. If the host bus 106 is a PCI-X bus, then each base address register is 32 bits wide if the base address register is an I/O decoder and 64 bits wide if the base address register is a memory decoder. In alternative embodiments the length of the base address registers may have a different number of bits.

29[] The logic of FIG. 4 describes specific operations occurring in a particular order. In alternative embodiments, certain of the logic operations may be performed in a different order, modified or removed. Morever, steps may be added to the above described logic and still conform to the described embodiments. Further, operations described herein may occur sequentially or certain operations may be processed in parallel. Yet further, operations may be performed by a single processing unit or by distributed processing units.

30[] The foregoing description of the preferred embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto. The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.

** Intel is a registered trademark of Intel Corporation. PowerPC is a registered trademark of IBM Corporation.

WHAT IS CLAIMED IS:

1. A method for controlling one or more I/O devices coupled to a local bus, comprising:

associating a local bus function with the one or more I/O devices;

configuring a register corresponding to the local bus function as a memory address; and

controlling the one or more I/O devices via the configured register.

2. The method of claim 1, wherein the memory address is coupled to a memory space, wherein the memory space maps control to the one or more I/O devices, and wherein the one or more I/O devices are controlled by accessing the memory space.

3. The method of claim 1, wherein the configuring is performed by configuration software coupled to the local bus.

4. The method of claim 1, wherein the register is configured as a memory base address register, and wherein the memory base address register is 32 bits or 64 bits long.

5. The method of claim 1, wherein the configured register functions as a programmable memory decoder.

6. The method of claim 1, wherein the register is stored in a configuration header of the local bus function.

7. The method of claim 1, wherein the local bus is a PCI bus and the local bus function is a PCI function.

8. The method of claim 1, wherein the one or more I/O devices are storage devices connected in a point-to-point mechanism to the local bus.

9. The method of claim 8, wherein the point-to-point mechanism is implemented by a serial ATA interface.

10. The method of claim 1, wherein the local bus function is used to control more than four I/O devices.

11. The method of claim 1, wherein the one or more I/O devices comply with the ATA, ATAPI or SATA interface.

12. A method for controlling one or more I/O devices connected to a local bus, comprising:

associating a local bus function with the one or more I/O devices;

if the one or more I/O devices are in a first access mode, configuring a register as an I/O address;

if the one or more I/O devices are in a second access mode, configuring the register corresponding to the local bus function as a memory address.

13. The method of claim 12, wherein the first access mode is a PCI IDE mode and the second access mode is a direct access mode.

14. The method of claim 12, wherein the register is stored in a configuration header of the local bus function, and wherein the register is configured as a memory decoder by configuring the register as a memory base address register.

15. The method of claim 12, wherein the register is stored in a configuration header of the local bus function, and wherein the register is configured as a I/O decoder by configuring the register as a I/O base address register.

16. A system for controlling one or more I/O devices coupled to a local bus, comprising:

a local bus function associated with the one or more I/O devices; and

a register corresponding to the local bus function, wherein the register is configured as a memory address, and wherein the one or more I/O devices are controlled via the configured register.

17. The system of claim 16, further comprising a host bus adapter, wherein the host bus adapter couples the one or more I/O devices to the local bus.

18. The system of claim 16, further comprising:

a memory space, wherein the memory address is coupled to the memory space, wherein the memory space maps control to the one or more I/O devices, and wherein the one or more I/O devices are controlled by accessing the memory space.

19. The system of claim 16, wherein the register is configured as a memory base address register, and wherein the memory base address register is 32 bits or 64 bits long, and wherein the configured register functions as a programmable memory decoder.

20. The system of claim 16, wherein the local bus is a PCI bus, wherein the local bus function is a PCI function, wherein the PCI function has a configuration header, and wherein the register is stored in the configuration header of the PCI function.

21. The system of claim 16, wherein the local bus function is used to control more than four I/O devices.

22. The system of claim 16, wherein the one or more I/O devices comply with the ATA, ATAPI or SATA interface.

23. A system comprising:

a local bus;

one or more I/O devices coupled to the local bus;

a local bus function associated with the one or more I/O devices; and

a register corresponding to the local bus function, wherein the register is configured as a memory address, and wherein the one or more I/O devices are controlled via the configured register.

24. The system of claim 23, further comprising a host bus adapter, wherein the host bus adapter couples the one or more I/O devices to the local bus.

25. The system of claim 23, further comprising:

a memory space, wherein the memory address is coupled to the memory space, wherein the memory space maps control to the one or more I/O devices, and wherein the one or more I/O devices are controlled by accessing the memory space.

26. The system of claim 23, further comprising:

configuration software coupled to the local bus, wherein the configuration software configures the register as the memory address.

27. The system of claim 23, wherein the register is configured as a memory base address register, and wherein the memory base address register is 32 bits or 64 bits long, and wherein the configured register functions as a programmable memory decoder.

28. The system of claim 23, wherein the one or more I/O devices are storage devices connected in a point-to-point mechanism to the local bus.

29. The system of claim 23, wherein the local bus function is used to control more than four I/O devices.

30. A system, comprising:

a local bus;

one or more I/O devices coupled to the local bus;

a local bus function associated with the one or more I/O devices; and

a register corresponding to the local bus function, wherein if the one or more I/O devices are in a first access mode the register is configured as an I/O address, and wherein if the one or more I/O devices are in a second access mode the register is configured as a memory address.

31. The system of claim 30, wherein the local bus function is a PCI function, wherein the first access mode is a PCI IDE mode, and wherein the second access mode is a direct access mode.

32. The system of claim 30, further comprising:

a configuration header coupled to the local bus function, wherein the register is stored in the configuration header, and wherein the register is configured as a memory decoder by configuring the register as a memory base address register.

33. The system of claim 30, further comprising:

a configuration header coupled to the local bus function, wherein the register is stored in the local bus function, and wherein the register is configured as a I/O decoder by configuring the register as a I/O base address register.

34. An article of manufacture for controlling one or more I/O devices coupled to a local bus, wherein the article of manufacture is capable of causing operations, the operations comprising:

associating a local bus function with the one or more I/O devices;

configuring a register corresponding to the local bus function as a memory address; and

controlling the one or more I/O devices via the configured register.

35. The article of manufacture of claim 34, wherein the memory address is coupled to a memory space, wherein the memory space maps control to the one or more I/O devices, and wherein the one or more I/O devices are controlled by accessing the memory space, and wherein the configuring is performed by configuration software coupled to the local bus.

36. The article of manufacture of claim 34, wherein the configured register functions as a programmable memory decoder, wherein the register is configured as a memory base address register, and wherein the memory base address register is 32 bits or 64 bits long.

37. The article of manufacture of claim 34, wherein the local bus is a PCI bus and the local bus function is a PCI function, and wherein the register is stored in a configuration header of the PCI function..

38. The article of manufacture of claim 34, wherein the local bus function is used to control more than four I/O devices.

39. The article of manufacture of claim 34, wherein the one or more I/O devices comply with the ATA, ATAPI or SATA interface.

40. An article of manufacture for controlling one or more I/O devices connected to a local bus, wherein the article of manufacture is capable of causing operations, the operations comprising:

associating a local bus function with the one or more I/O devices;

if the one or more I/O devices are in a first access mode, configuring a register as an I/O address; and

if the one or more I/O devices are in a second access mode, configuring the register corresponding to the local bus function as a memory address.

41. The article of manufacture of claim 40, wherein the first access mode is a PCI IDE mode and the second access mode is a direct access mode.

42. The article of manufacture of claim 40, wherein the register is stored in a configuration header of the local bus function, and wherein the register is configured as a memory decoder by configuring the register as a memory base address register.

43. The article of manufacture of claim 40, wherein the register is stored in a configuration header of the local bus function, and wherein the register is configured as a I/O decoder by configuring the register as a I/O base address register.

FIG. 1

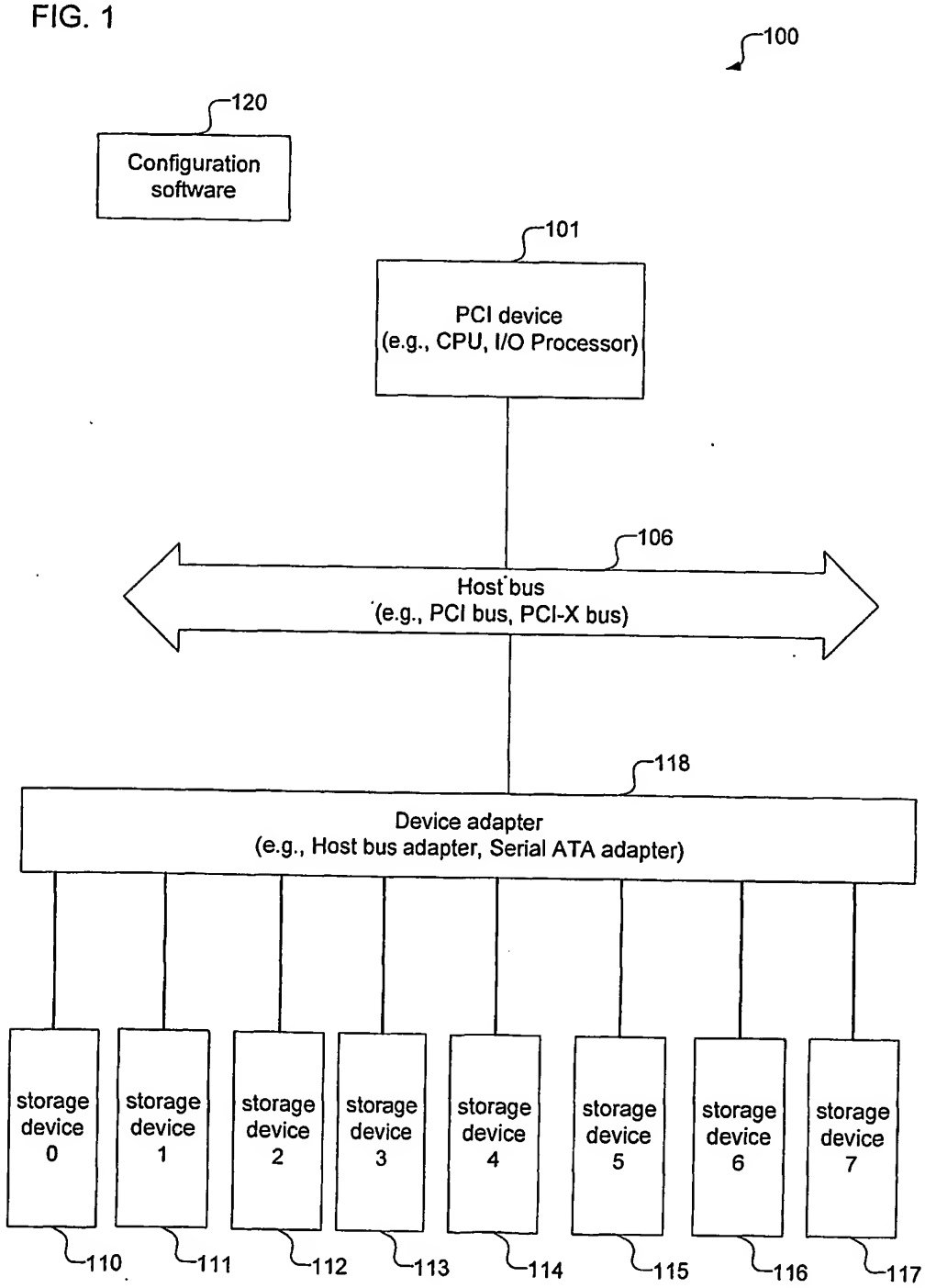

100
120
Configuration software
101
PCI device (e.g., CPU, I/O Processor)
106
Host bus (e.g., PCI bus, PCI-X bus)
118
Device adapter (e.g., Host bus adapter, Serial ATA adapter)
storage device 0
storage device 1
storage device 2
storage device 3
storage device 4
storage device 5
storage device 6
storage device 7
110
111
112
113
114
115
116
117

FIG. 2

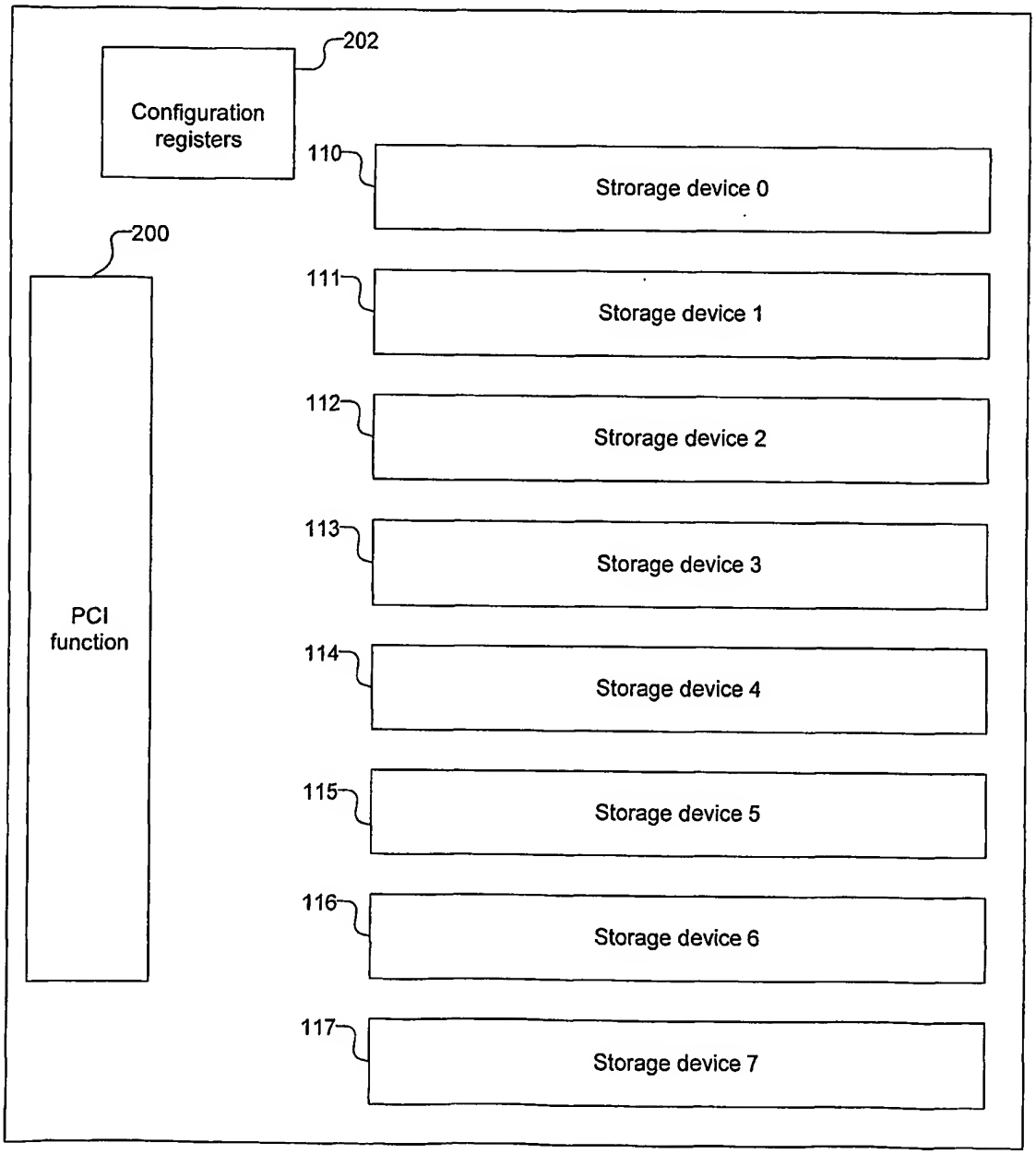

202
Configuration registers
110
Strorage device 0
200
111
Storage device 1
112
Strorage device 2
113
Storage device 3
PCI function
114
Storage device 4
115
Storage device 5
116
Storage device 6
117
Storage device 7

FIG. 3

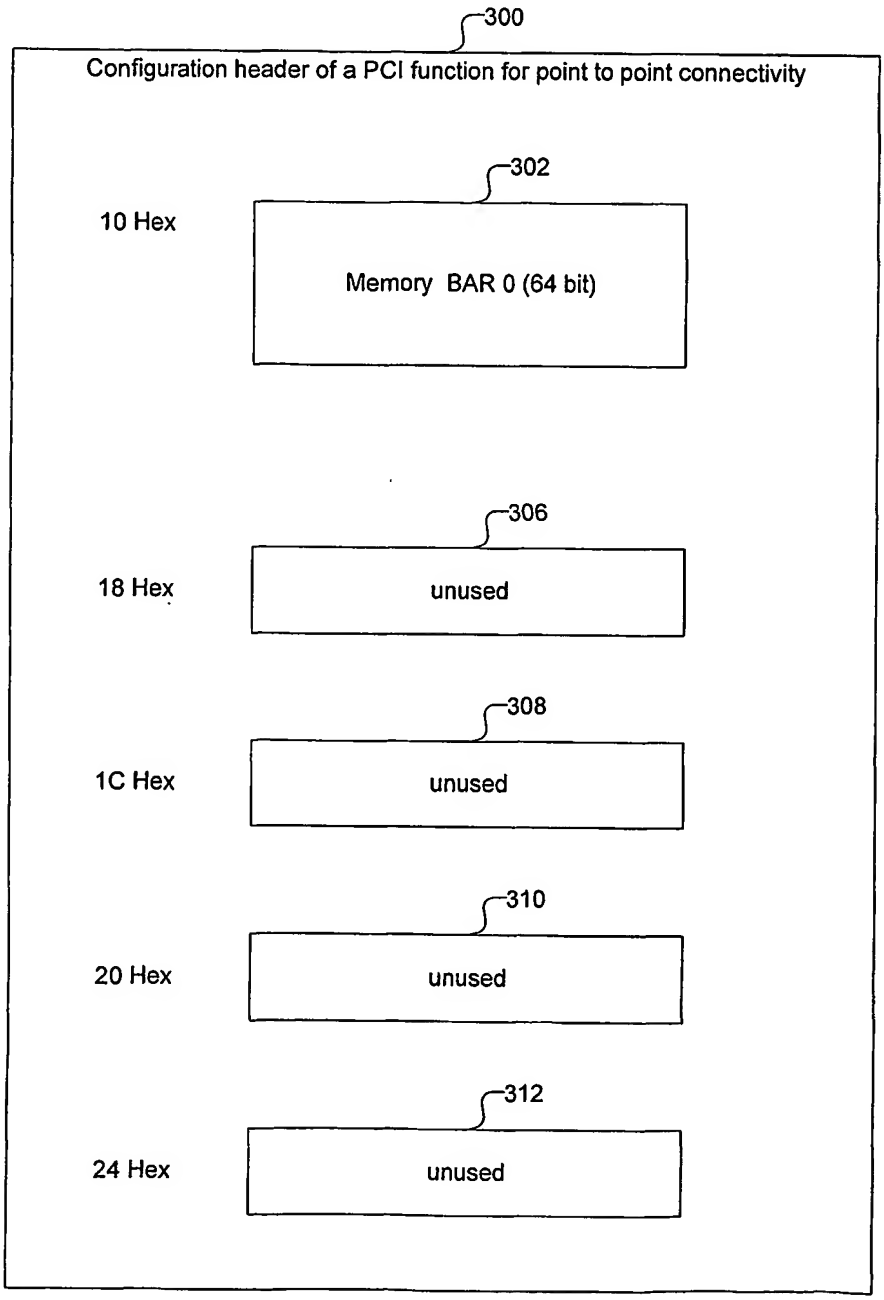
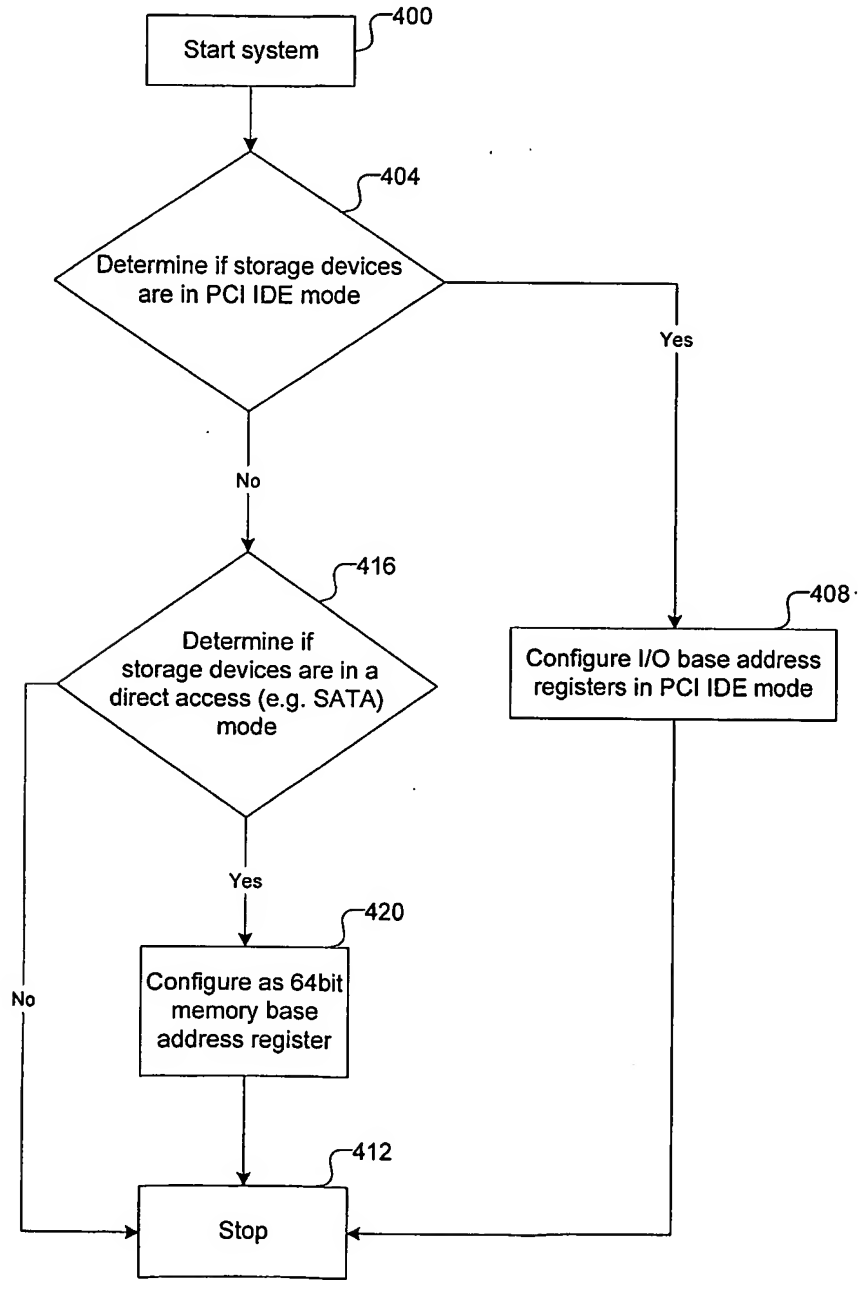

300
Configuration header of a PCI function for point to point connectivity
302
10 Hex
Memory BAR 0 (64 bit)
306
18 Hex
unused
308
1C Hex
unused
310
20 Hex
unused
312
24 Hex
unused

FIG. 4


Start system
400
Determine if storage devices are in PCI IDE mode
404
Yes
No
Configure I/O base address registers in PCI IDE mode
408
Determine if storage devices are in a direct access (e.g. SATA) mode
416
Yes
No
Configure as 64bit memory base address register
420
Stop
412

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/22943

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F13/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 838 932 A (ALZIEN KHALDOUN) 17 November 1998 (1998-11-17) abstract column 2, line 41 -column 3, line 7 column 13, line 48 -column 14, line 42 ---	1
X	US 6 233 641 B1 (LAMBETH SHAWN MICHAEL ET AL) 15 May 2001 (2001-05-15) abstract column 1, line 58 -column 2, line 9 column 2, line 25 -column 3, line 40 column 5, line 5 - line 67 column 12, line 6 - line 43 figures 1,2B -----	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 December 2003	23/12/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Rudolph, S

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 03/22943

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 2-43
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Claims Nos.: 2-43

The initial phase of the search revealed a very large number of documents relevant to the issue of novelty. So many documents were retrieved that it is impossible to determine which parts of the claim(s) may be said to define subject-matter for which protection might legitimately be sought (Article 6 PCT):

A method for controlling one or more I/O devices coupled to a local bus, comprising:
associating a local bus function with the one or more I/O devices;
configuring a register corresponding to the local bus function as a memory address; and
controlling the one or more I/O devices via the configured registe (under this scope falls each PCI-bridge which maps devices coupled a secondary bus to the logical address space of a primary bus, the usage of a register in order to associate a memory address is implicit; see 'US5838932, abstract and column 13/line 48-column 14/line 11! and 'US6233641, abstract and column 1/line 58-column 2/line 9!).

For these reasons, a meaningful search over the whole breadth of the claim(s) is impossible. Consequently, the search has been restricted to claim 1.

The applicant's attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 03/22943

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5838932 A	17-11-1998	US 5809435 A	15-09-1998
		US 5802324 A	01-09-1998
		JP 11085674 A	30-03-1999
		SG 65758 A1	22-06-1999
US 6233641 B1	15-05-2001	NONE	